REMARKS

Section A lists the current status of the claims. Sections B and C address the claim rejections in the order in which they appear in the Action of May 2, 2006.

A. Status of the Claims

Claims 1-11 are pending in the application. Claims 1-2 and 4-11 were rejected under 35 USC 102(b) as being anticipated by Noguchi, US Patent No. 6,005,270. Claim 3 was rejected under 35 USC 103(a) as being unpatentable over Noguchi in view of Walker, US Patent No. 6,593,624.

B. 35 USC 102(b) Rejections: Claims 1-2 and 4-11

Claims 1-2 and 4-11 were rejected under 35 USC 102(b) as being anticipated by Noguchi.

Claim 1 has been amended to recite an array of thin film transistors comprising polysilicon, wherein the polysilicon is formed by a method comprising: depositing a first layer of amorphous silicon; depositing silicon nuclei on the first layer of amorphous silicon; depositing a second layer of amorphous silicon over the first layer and the nuclei, wherein conversion of the first layer to hemispherical grains before deposition of the second layer is substantially prevented; and annealing the first and second layers of amorphous silicon to induce crystallization.

Claim 5 recites a monolithic three dimensional memory array comprising memory cells, said memory cells comprising polysilicon, any of said polysilicon crystallized by a method comprising: embedding deposited silicon nuclei between layers of amorphous silicon; and crystallizing from the embedded silicon nuclei.

Claim 8 has been amended to recite an array of thin film transistors comprising channel regions, the channel regions formed by a method comprising: embedding deposited silicon nuclei between layers of amorphous silicon; and annealing the nuclei and amorphous silicon layers.

All three independent claims, 1, 5, and 8, recite an array of memory cells or transistors, each memory cell or transistor including a film, the film made by a method different than the methods describe by Noguchi (laser anneal and conventional solid phase crystallization). The Examiner apparently maintains that the product of Noguchi and the product of the present invention are the same, even though made by a different process.

Applicant will show that the different process used to create the claimed arrays and the array of Noguchi result arrays which are not identical, and in fact are structurally distinct.

Noguchi teaches an array of thin film transistors, each having a polysilicon channel region 31b (Fig. 5d – Fig. 10.) Noguchi teaches to deposit silicon layer 31a as amorphous silicon and to crystallize it using an "ELA process", or Excimer laser anneal (col. 12, line 56 – col. 13, line 14.) Alternatively, in some embodiments, Noguchi teaches crystallizing silicon layer 31b using a conventional solid phase crystallization method (col. 13, lines 12-14.)

An array formed in a film crystallized by laser anneal is structurally distinct

During a laser anneal, a laser beam scans an amorphous film to be crystallized. The silicon crystals grow oriented relative to the path of the laser beam. Silicon crystals grown using the methods described in the present application grow outward from

embedded nuclei (see paragraphs [0023], [0031], and [0040] of the present application.) The method of the present invention creates a highly uniform film, while a film crystallized by an ELA process will be highly non-uniform, depending on the path and extent of the beam. Thus the shape and distribution of silicon crystals making up a polysilicon film will be different in a film crystallized by an ELA process (as in Noguchi) and by the processes described in the present invention.

As the number and orientation of grain boundaries strongly influences carrier mobility, which in turn strongly influences cell behavior, the qualities of a cell will differ significantly depending on its placement and orientation relative to silicon crystals in the polysilicon film. For example, the device channel may be oriented along the direction of laser scan, thus minimizing the number of grain boundaries in the channel, improving mobility and thus improving device performance. Alternatively, the channel can be oriented at ninety degrees to the direction of laser scan, maximizing the number of grain boundaries in the channel. In the present invention, the silicon nuclei are randomly distributed, and orientation of the channel region cannot be selected to affect device performance.

Thus across the *array* of transistors described by Noguchi, the placement and orientation of each transistors will strongly influence its performance. Transistors will need to be carefully placed to optimize their location relative to the highly non-uniform distribution of silicon crystals. Alternatively, the transistors of Noguchi may be placed and oriented *without* regard to the distribution of silicon crystals, but in this case device performance and quality will vary widely across the array.

In the claimed array, in contrast, because the crystallization method recited forms a highly uniform film, transistors can be placed randomly at any point in the film without location and orientation systematically affecting device performance.

Applicants thus respectfully assert that the array of Noguchi will not be identical to the claimed array. The array of Noguchi will either require careful selective placement and orientation of transistors making up the array, or, if the transistors are not so placed and oriented, the performance of transistors will vary widely across the array. The claimed array need not be selectively placed, and performance of devices will not differ markedly across the array. The array of Noguchi and the claimed array are not structurally the same.

An array formed in a film crystallized by conventional SPC is structurally distinct

Noguchi also mentions conventional solid phase crystallization (SPC) as a possible means to crystallize film 31b. As described in the present application, nucleation sites form during SPC, and hemispherical grains tend to form around these nucleation sites, forming a rough, uneven surface (paragraphs [0021]-[0023].) The methods of the present invention prevent such an uneven surface. An uneven surface increases variability across a memory array, which is undesirable.

The array of Noguchi, then, is formed in a film having a rough surface, increasing undesirable variability across the array; in array recited in claims 1, 5, and 8, the method of formation guarantees that no such roughness, or consequent variability across the array, exists. These arrays are structurally distinct.

Thus the polysilicon of the memory cells, and the memory array comprising those memory cells, of the present invention has distinct characteristics because of the method

used to crystallize this polysilicon. This different character causes these devices, and this array, to have a different structure and to behave differently. For this reason claims 1-2 and 4-11 distinguish over Noguchi.

Applicants respectfully request reconsideration.

C. 35 USC 102(b) Rejections: Claim 3

Claim 3 was rejected under 35 USC 103(a) as being unpatentable over Noguchi in view of Walker. Claim 3 indirectly depends from claim 1, and thus distinguishes over the references for the reasons described in Section B of these remarks.

CONCLUSION

In view of the preceding Remarks, Applicant submits that this application is in condition for allowance. Reconsideration is respectfully requested. If objections remain, Applicant **respectfully requests an interview.** In the event that objections remain, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

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Date

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